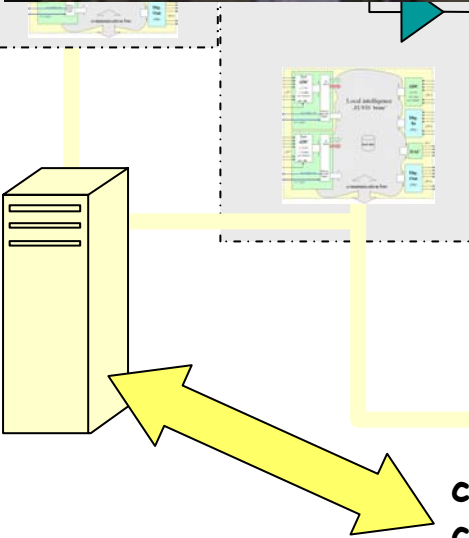


# The „ELWIS“-concept of MHF-e for PETRA-III



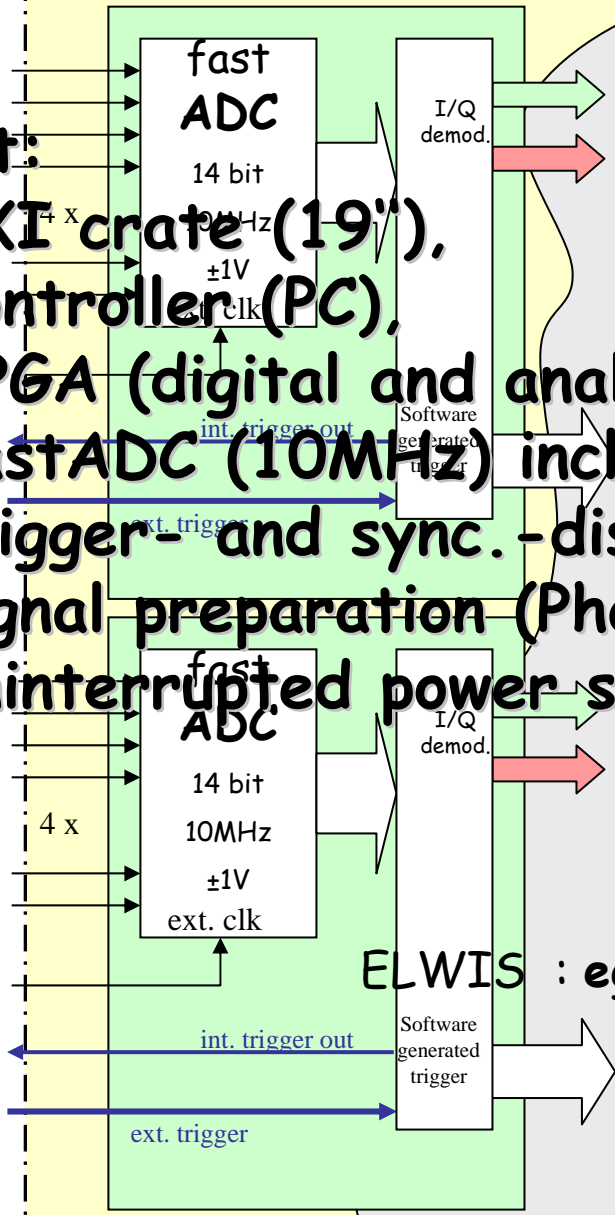
kit:

PXI crate (19"),  
controller (PC),  
FPGA (digital and analog in-/outputs),

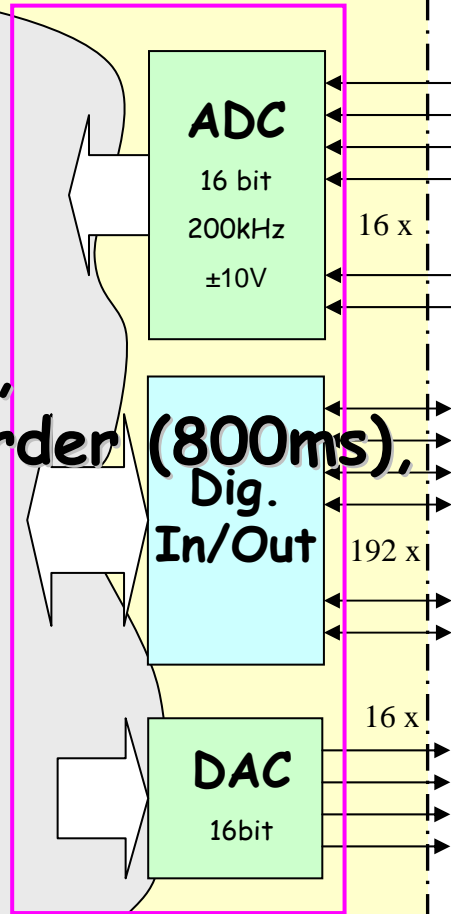
fastADC (10MHz) incl. transient recorder (800ms),  
trigger- and sync.-distribution,

signal preparation (Phoenix),  
uninterrupted power supply

local intelligence  
„ELWIS' brain“



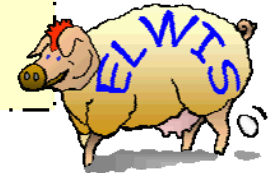
hard disk  
Compact Flash



2 FPGA  
NI 7831R PXI

ELWIS : egg laying wool milk sow

communication



ALARM RST ALARM TEMP 3.3V 5V +12V -12V

ELWIS25

trigger and sync

2	3
ELWIS	ELWIS
FAST-ADC	FAST-ADC
CH1	CH1
FPGA1 FPGA2	FPGA1 FPGA2
CH2	CH2
CH3	CH3
TRIG RST	TRIG RST
CH4	CH4
DES FEA	DES FEA

NATIONAL INSTRUMENTS  
NI PXI-7831R  
Reconfigurable I/O

ADLINK TECHNOLOGY INC.

Compact

1. FPGA

2. FPGA

PXI PXI



# implementation I

- 28 ELWIS-moduls (PXI crates, 19 inch)
- Microsoft Windows XP
- LabVIEW (LV) 8.0 from National Instruments (NI)
- programming of NI-FPGA-cards in LabVIEW (no VHDL-knowledge necessary!)
- communication in TINE (ethernet)
- each ELWIS module differ only in software (modularity, CF)
- radiationtest in DORIS (one FPGA fault at 45 Gy)
- control of stepper motors (tuner in cavity) implemented in FPGA code written by us
- the 8 channels of fast ADC (10MHz I/Q) includes transientrecorders (800ms)



# implementation II

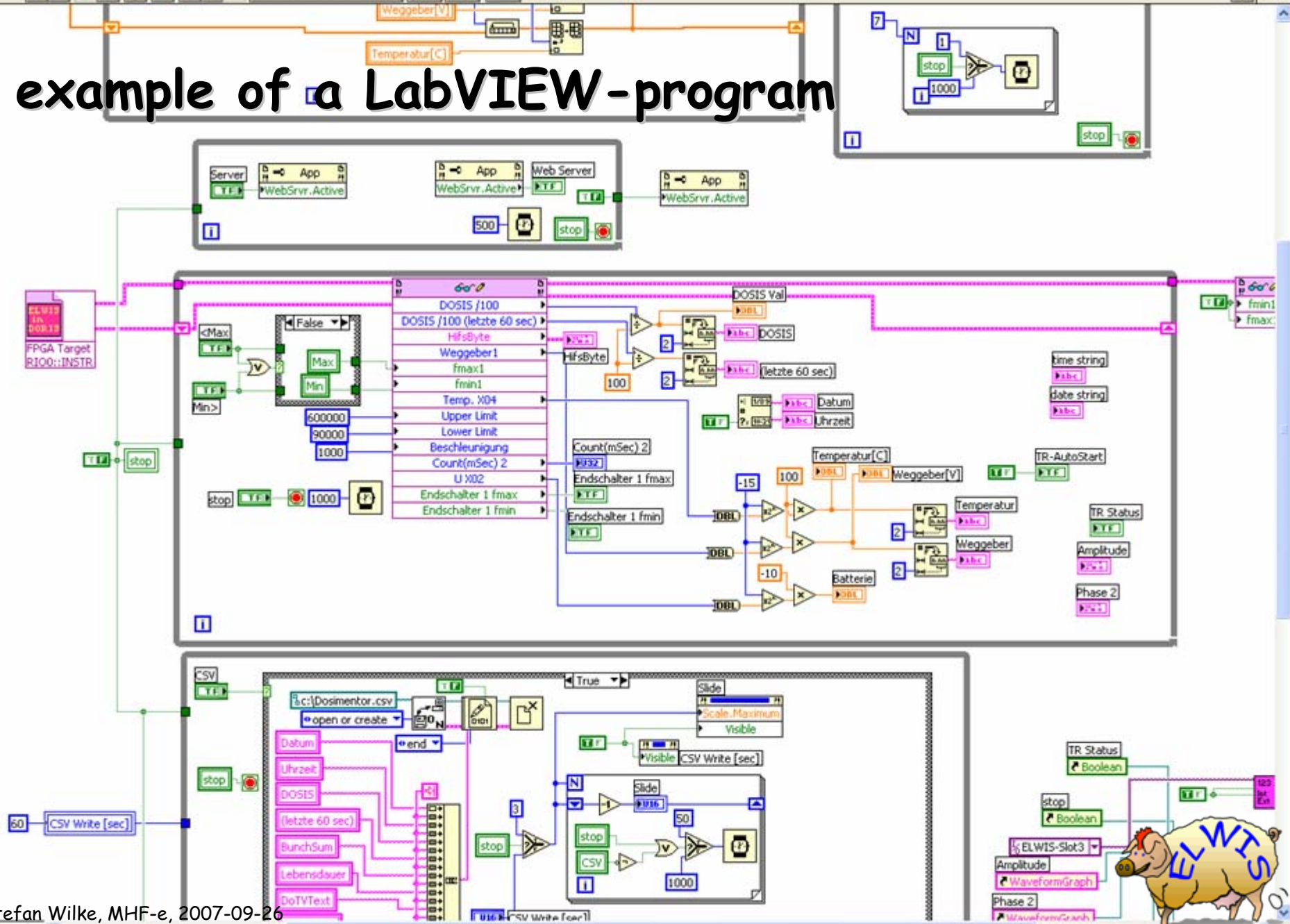
- LV is a simple graphic software running in data flow model, at DESY in many groups often used. Without spezial knowledge we reach in teams of many colleagues (no computer scientist, but technician and engineers) pragmatic results.
- Very good TINE support at DESY. Many TINE-VIs ready for LabVIEW.
- number of signals: ca. 1000

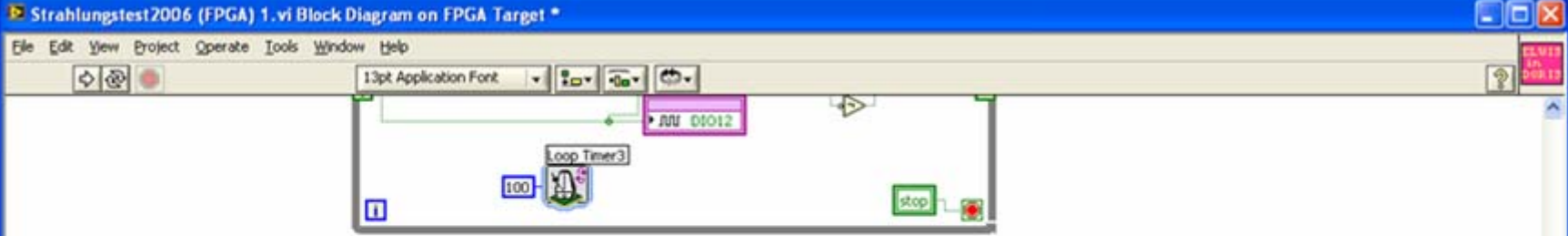
security: paranoid - naive - isolated net.  
 authorization of active switching will manage TINE  
 stability:  
 example: since 2007-03-21 in DORIS-tunnel  
<http://mhfexpelwis03.desy.de/Dosimentor.html>

Anzahl pro Sender	6	2	2	1	1	1	1	Summe
ELWIS	ELWIS	Modulstron	Modulstron	Sender	Post	Verteilung	HF-Regelung	
Fast Analog Eingänge :	7	5	5	8	0	8	6	84
Analog Eingänge :	16	4	13	8	0	2	2	142
Digital Out :	0	2	4	0	0	0	2	14
Digital Eingänge :	12	0	12	10	8	2	3	119
Digital Ausgänge :	11	4	12	4	0	0	4	106
pro ELWIS	46	15	46	30	8	12	17	165
pro Typ bei 1 Sender	276	30	92	70	12	17	17	930
Gesamtanlage								

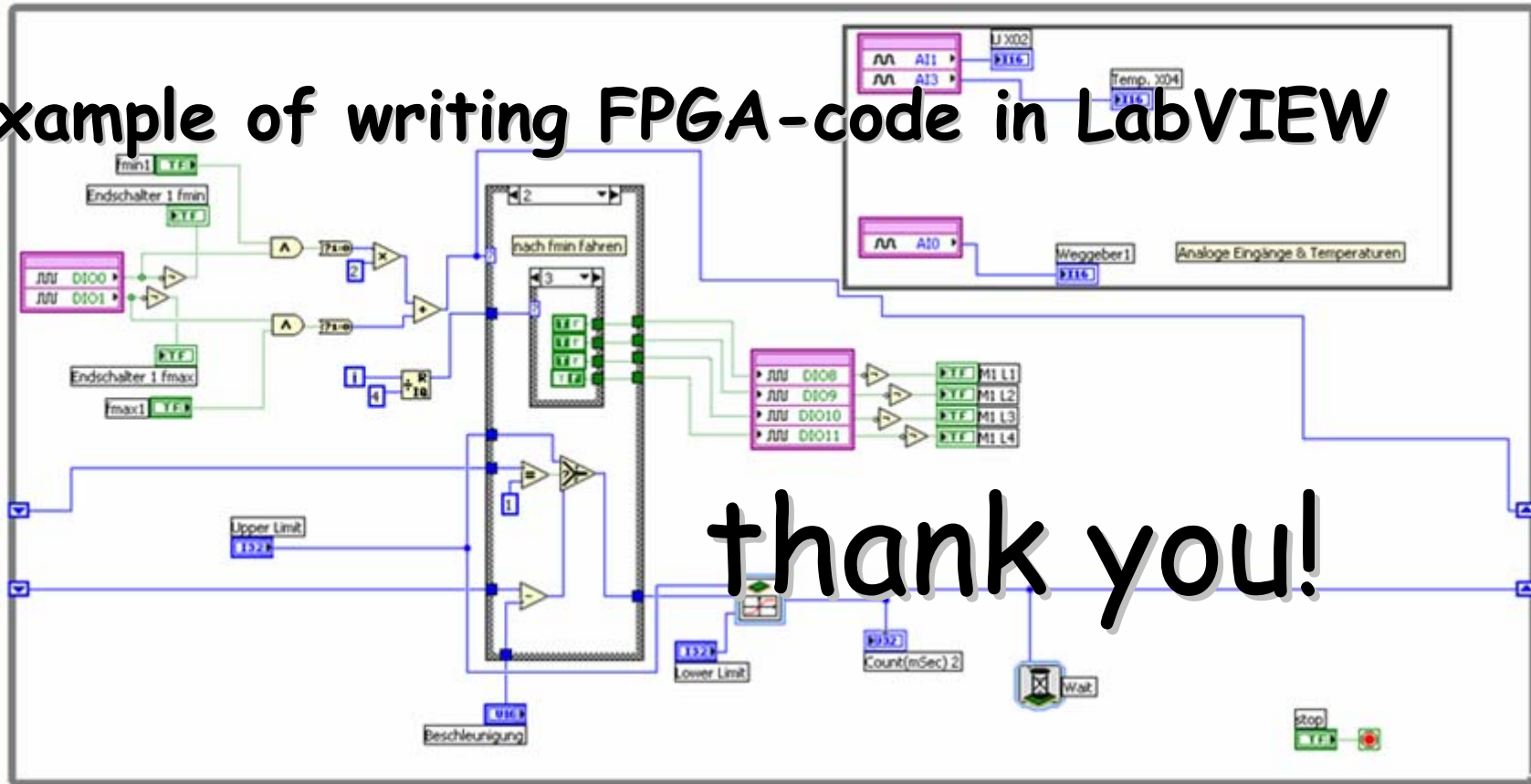


# example of a LabVIEW-program





example of writing FPGA-code in LabVIEW



thank you!



# fast ADC card





# test of a cavity-ELWIS

